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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/808,367	03/15/2001	Yuichi Koga	05225.0196	3413

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FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
1300 I STREET, NW
WASHINGTON, DC 20005

EXAMINER	
PHAN, RAYMOND NGAN	
ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/808,367	KOGA, YUICHI	
	Examiner	Art Unit	
	Raymond Phan	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

1. This action is responsive to the following communications: RCE filed on August 04, 2004.

2. This application has been examined. Claims 1-14 are pending.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 9 and 12 are rejected under 35 U.S.C. § 102(e) as being anticipated by Applicants Admitted Prior Arts (hereinafter AAPA).

In regard to claim 9, AAPA discloses providing an on-board memory area including at least one on-board type memory module in the electronic equipment (see figure 5, page 2); providing a slot-type memory area including at least one memory slot, each memory slot being coupled to the on-board memory in series (see figure 5, page 2); installing at least one slot-type memory module in the at least one memory slot (see figure 5, page 2); and providing a memory controller,

coupled in series to the on-board memory and slot-type memory, that controls access to the on-board and slot-type memory modules (see figure 5, page 2).

In regard to claim 12, AAPA discloses an on-board type memory module installed on a board (see figure 5, page 2); at least one memory slot provided on the board the memory slot coupled in series to the on-board type memory module (see figure 5, pages 2-3); a memory controller, coupled in series to the on-board type memory module and the at least one memory slot (see figure 5, page 2).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-8, 10-11, 13-14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants Admitted Prior Arts (hereinafter AAPA) in view of Wu (US Pub No. 2001/0003198).

In regard to claims 1, 13, 14, AAPA discloses the electronic equipment comprising a board including an on-board memory for installing memory modules, and a slot-type memory area for installing slot-type memory modules (see figure 5, pages 2); at least one on-board type memory module installed in the on-board memory area (see figure 5, page 2); at least one slot-type memory module installed in the slot-type memory area, each memory slot coupled in series to the on-board memory modules (see figure 5); at least one slot-type memory module installed in the slot-type memory area (see figure 5, pages 2-3), each slot-type memory module

having a specified operating frequencies (i.e. 66MHZ or 100MHZ) (see figure 5, page 1); a memory controller coupled in series to the on-board memory and slot-type memory modules (see figure 5, pages 2-3); a memory bus that couples to the memory controller to the on-board memory and slot-type memory modules in series (see figure 5, pages 2-3). But AAPA does not specifically disclose the memory controller providing access using a designated operating frequencies. However Wu discloses the plurality of memory modules having plurality of operating frequencies (see paragraphs 0029-0032). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Wu within the system of Coteus et al. because it would result in optimal memory performance.

In regard to claim 2, Wu discloses the frequency controller that designates the operating frequency of the memory bus (see paragraphs 0029-0030). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Wu within the system of AAPA because it would result in optimal memory performance.

In regard to claims 3, 6, Wu discloses designates the specified operating frequency of the slot-type memory modules as the operating frequency for both the on-board memory and slot-type memory modules when the operating frequency of the on-board memory module is different from the operating frequency of the slot-type memory module (see paragraphs 0034-0040). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Wu within the system of AAPA because it would result in optimal memory performance.

In regard to claims 4, 7, Wu discloses designates the specified operating frequency of the on-board memory modules as the operating frequency for both the on-board memory and slot-type memory modules when the operating frequency of the on-board memory module is different from the operating frequency of the slot-type memory module (see paragraphs 0034-0040). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Wu within the system of AAPA because it would result in optimal memory performance.

In regard to claim 5, Wu discloses an input mechanism (i.e. registers) designating whether to use the specified operating frequency of the on-board memory module or the slot-type memory module, when the operating frequency of the on-board memory module is different than the operating frequency of the slot-type memory module (see paragraphs 0034-0040). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Wu within the system of AAPA because it would result in optimal memory performance.

In regard to claim 8, even though the teachings of AAPA or Wu do not specifically disclose the notification to the user when the memory controller detects the defective (i.e. different operating frequencies), however one skilled in the art would have understood that they can choose to implement the notification display to fulfill their need.

In regard to claim 10, Wu discloses the step of determining whether a defective memory module (i.e. SPD) based on the attribute information on the respective on-board and slot-type memory modules (see paragraphs 0028-0030); and controlling start-up operation of the equipment based on the determination (see

paragraph 0031). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Wu within the system of AAPA because it would result in optimal memory performance.

In regard to claim 11, AAPA discloses providing an on-board memory area including at least one on-board type memory module in the electronic equipment (see figure 5, page 2); providing a slot-type memory area including at least one memory slot, each memory slot being coupled to the on-board memory in series (see figure 5, page 2); installing at least one slot-type memory module in the at least one memory slot (see figure 5, page 2); and providing a memory controller, coupled in series to the on-board memory and slot-type memory, that controls access to the on-board and slot-type memory modules (see figure 5, page 2). But AAPA does not disclose the reading the attribute information of the on-board type and slot-type memory modules and determining whether a defective memory module (i.e. SPD) based on the attribute information on the respective on-board and slot-type memory modules. However Wu discloses the reading the attribute information of the on-board type and slot-type memory modules (see paragraphs 0029-0029) and determining whether a defective memory module (i.e. SPD) based on the attribute information on the respective on-board and slot-type memory modules (see paragraph 0030). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Wu within the system of AAPA because it would result in optimal memory performance.

Response to Amendment

7. Applicant's arguments, see pages 9-13, filed on August 4, 2004, with respect

to the rejections of claims 1-12 under 35USC103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of AAPA and Wu.

Conclusion

8. All claims are rejected.

9. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.

Fischer et al. (US No. 5,239,639) disclose an efficient memory controller with an independent clock.

Bonella (US No. 5,333,293) disclose a multiple input frequency memory controller.

Mamata (US No. 6,792,561) discloses an apparatus and method for controlling access to expansion memory for a computer system.

Fukushima et al. (US No. 5,727,182) disclose a method and apparatus for adjusting output current values for expansion memories.

Bruce, II et al. (US No. 5,566,325) disclose a method and apparatus for adaptive memory access.

Lee (US No. 6,530,001) discloses a computer system controlling memory clock signal and method for controlling the same.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (703) 306-2756. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Primary, Paul Myers can be reached on (703) 305-9656 or via e-mail addressed to paul.myers@uspto.gov. The fax phone number for this Group is (703) 872-9306.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to **[raymond.phan@uspto.gov]**.

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

PAUL R. MYERS
PRIMARY EXAMINER

Raymond Phan
10/10/04